# *Adjustable Current-Limit Single-Channel Power Distribution Switch*

## Description

FP6861E-A/B is a cost-effective, low voltage, single N-Channel MOSFET high-side power switch, optimized for self-powered and bus-powered Universal Serial Bus (USB) applications.

FP6861E-A/B is equipped with a charge pump circuitry to drive the internal MOSFET switch. The switch's low $R_{DS(ON)}$ meets USB voltage drop requirement, and a flag output is available to indicate fault conditions to the local USB controller. FP6861E-A/B also provides adjustable current limit threshold between 0.12~1.7A through an external resistor.

Additional features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, and under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present. Besides, fault current is limited to specific current for FP6861E-A/B in single port in accordance with the USB power requirements. FP6861E-A/B will prevent reverse current with reverse voltage protection.

FP6861E-A/B is available in SOT-23-6 and TDFN-6 (2mm×2mm) packages with smallest components.

## Features

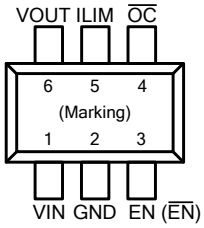
- Compliant to USB Specifications
- Adjustable Current Limit: 0.12~1.7A
- Accurate Current-Limit：±6% at 1.7A
- Built-in Low $R_{DS(ON)}$ N-Channel MOSFET
- Output can be Forced Higher than Input
- Low Supply Current:
  120μA Typical at Switch On State ($R_{ILIM}$=20kΩ)
  0.1μA Typical at Switch Off State
- Wide Input Voltage Ranges: 2.7V to 6V
- Open-Drain Fault Flag Output
- Hot Plug-In Application (Soft-Start)
- 2.2V Typical Under-Voltage Lockout (UVLO)
- Current Limit Protection
- Thermal Shutdown Protection
- Reverse Current Flow Blocking (No Body Diode)
- Reverse Voltage Protection
- Logic Level Enable Pin
- SOT-23-6 and TDFN-6 (2mm×2mm) Packages
- RoHS Compliant
- UL NO.E322418 (Approved model: FP6861 series)
- CB Test Certified, Ref. Certif. No. JPTUV-056846

## Applications

- USB Bus/Self Powered Hub
- USB Peripheral
- ACPI Power Distribution
- Notebook, Motherboard PC
- Battery-Charger Circuit

## Pin Assignments

**S6 Package (SOT-23-6)**




**WD Package (TDFN-6) (2mm×2mm)**

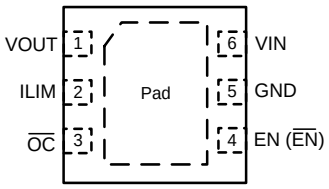



Figure1. Pin Assignment of FP6861E-A/B

## Ordering Information

FP6861E-□□□□□□

- TR: Tape/Reel
- C: Green
- Package Type
  S6: SOT-23-6
  WD: TDFN-6 (2mm×2mm)
- Enable Type
  1: Active High
  2: Active Low
- Current Limit Protection Type
  A: Constant-Current
  B: Latch-Off

**SOT-23-6 Marking**

| Part Number | Product Code |
|---|---|
| FP6861E-A1S6CTR | Fi5 |
| FP6861E-A2S6CTR | Fi6 |
| FP6861E-B1S6CTR | FF9 |
| FP6861E-B2S6CTR | FG1 |

**TDFN-6 (2mm×2mm) Marking**

| Part Number | Product Code |
|---|---|
| FP6861E-A1WDCTR | Fi7 |
| FP6861E-A2WDCTR | Fi8 |
| FP6861E-B1WDCTR | FG2 |
| FP6861E-B2WDCTR | FG3 |

## Typical Application Circuit

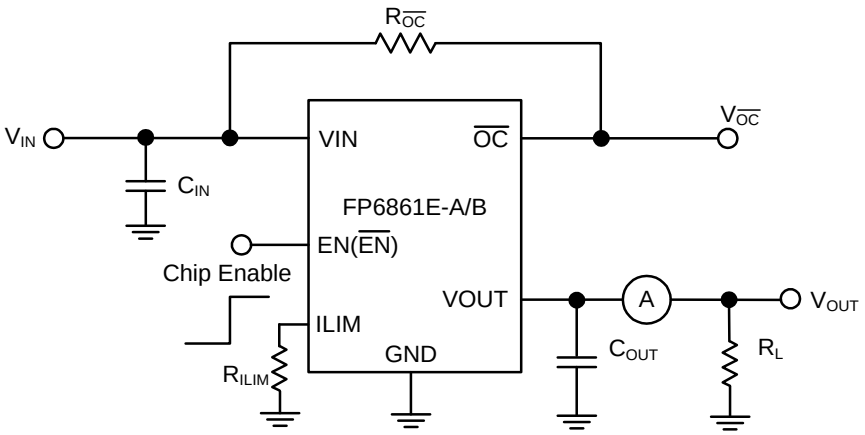
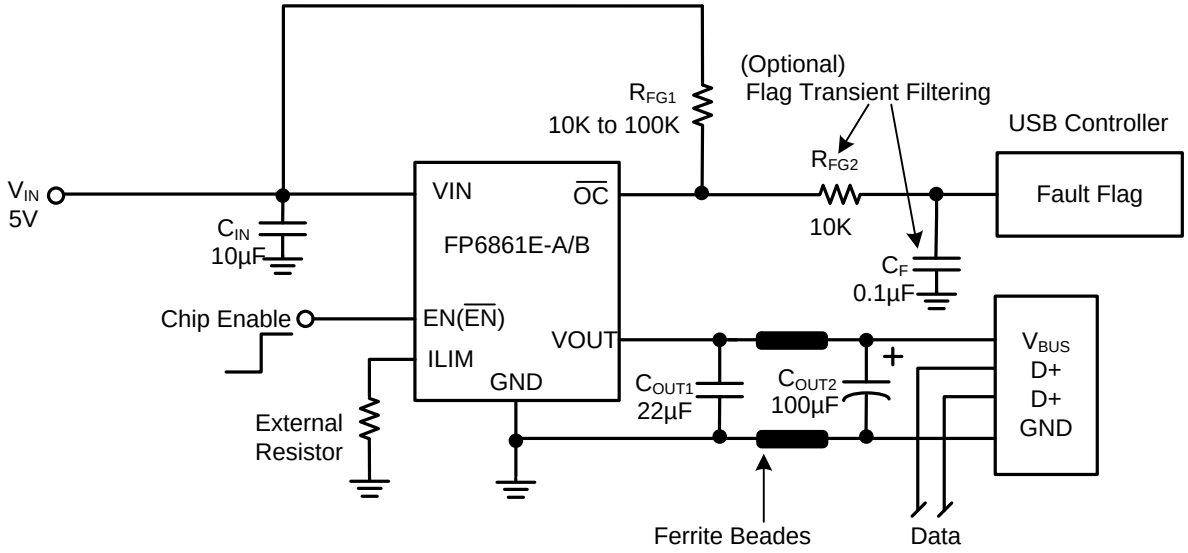



Figure 2. Electrical Characteristic Test Circuit




*Note: In most applications, adding one 1µF capacitor is enough. If the trace to VIN is long in PCB, placing larger input capacitor is needed.

Figure 3. Typical Application Circuit for USB Power Switch

## Functional Pin Description

| Pin Name | Pin No. (SOT-23-6) | Pin No. (TDFN-6) | Pin Function |
|---|---|---|---|
| **VIN** | 1 | 6 | Input Power Supply. |
| **GND** | 2 | 5 | Ground. Connect GND to exposed pad. |
| **EN/$\overline{\text{EN}}$** | 3 | 4 | Chip Enable/Chip Shutdown. Pull the pin high to enable IC; Pull the pin low to shutdown IC. Do not let the pin floating. |
| **$\overline{\text{OC}}$** | 4 | 3 | Fault Flag. Open-Drain Output. |
| **ILIM** | 5 | 2 | Use external resistor to set current-limit; recommended 15kΩ≦$R_{ILIM}$≦235kΩ |
| **VOUT** | 6 | 1 | Switch Output. |

## Block Diagram

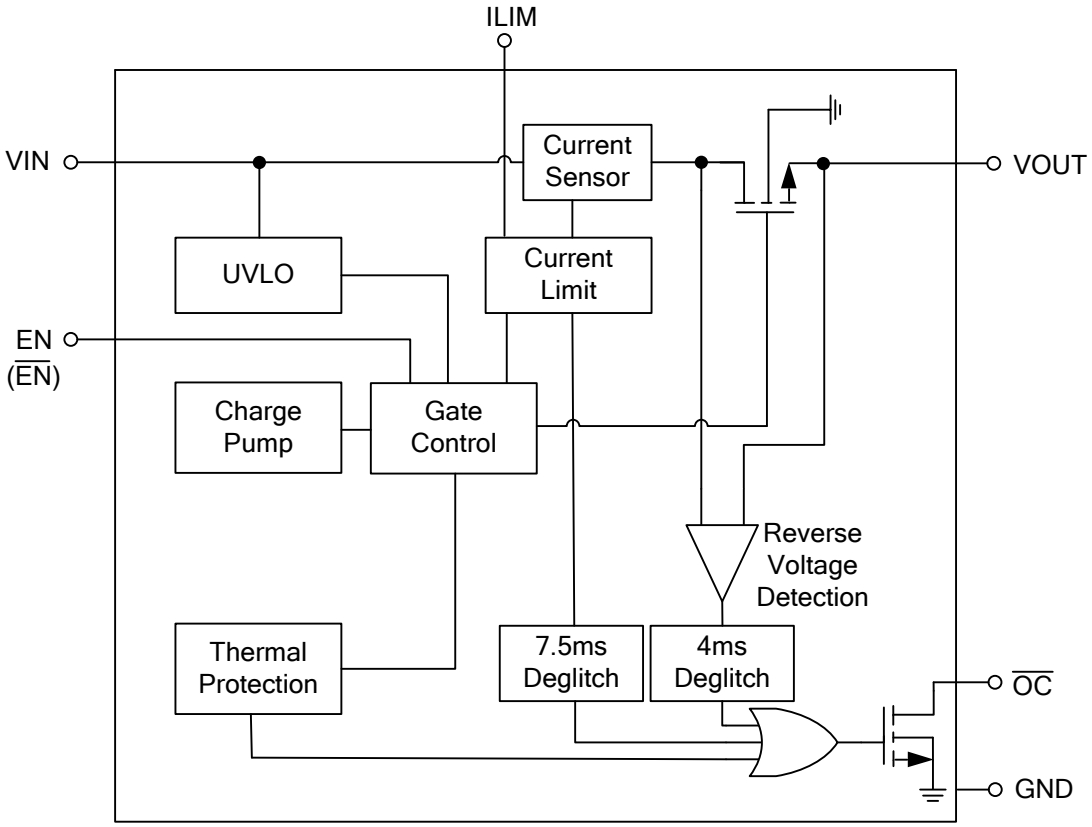



Figure 4. Block Diagram

## Absolute Maximum Ratings

- VIN, VOUT ---------- -0.3V to +7V
- All Other Pins Voltage---------- -0.3V to +7V
- Power Dissipation @$T_A$=25°C, ($P_D$)
  - SOT-23-6 ---------- +0.4W
  - TDFN-6 (2mm×2mm) ---------- +0.74W
- Package Thermal Resistance, ($\theta_{JA}$)
  - SOT-23-6 ---------- +250°C/W
  - TDFN-6 (2mm×2mm) ---------- +136ºC/W
- Package Thermal Resistance, ($\theta_{JC}$)
  - SOT-23-6 ---------- +110°C/W
  - TDFN-6 (2mm×2mm) ---------- +56ºC/W
- Junction Temperature ---------- +150°C
- Lead Temperature (Soldering,10 sec.) ---------- +260°C
- Storage Temperature Range ---------- -65°C to +150°C

Note 1：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

## Recommended Operating Conditions

- Supply Voltage ($V_{IN}$) ---------- +2.7V to +6V
- Junction Temperature---------- -40°C to +125°C
- Operation Temperature Range ($T_{OPR}$) ---------- -40°C to +85°C

## Electrical Characteristics

($V_{IN}$=5V, $T_A$=25°C, unless otherwise specified.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Switch On Resistance | $R_{DS(ON)}$ | $I_{OUT}$=500mA (SOT-23-6) | | 100 | | mΩ |
| | | $I_{OUT}$=500mA (TDFN-6) | | 85 | | |
| Supply Current | $I_{SW\_ON}$ | $R_{ILIM}$=20kΩ | | 120 | | μA |
| | $I_{SW\_OFF}$ | Switch OFF, $V_{OUT}$=Open | | 0.1 | 1 | |
| EN Threshold | $V_{IH}$ | Switch ON | 1.8 | | | V |
| | $V_{IL}$ | Switch OFF | | | 0.7 | |
| EN Input Current | $I_{EN}$ | $V_{EN}$=Enable | | 0.01 | 0.1 | μA |
| Current Limit | $I_{LIM}$ | $R_{ILIM}$=15kΩ | 1600 | 1700 | 1800 | mA |
| | | $R_{ILIM}$=20kΩ | 1215 | 1295 | 1375 | |
| | | $R_{ILIM}$=210kΩ | 95 | 125 | 150 | |
| Output Leakage Current | $I_{LEAKAGE}$ | $V_{EN}$=Disable, $R_L$=0Ω | | 0.5 | 1 | μA |
| Output Turn-On Rise Time | $T_{ON\_RISE}$ | $R_{ILIM}$=20kΩ, $C_L$=1μF | | 1 | | ms |
| $\overline{OC}$ Output Resistance | $R_{\overline{OC}}$ | $I_{SINK}$=1mA | | 70 | | Ω |
| $\overline{OC}$ Off Current | $I_{\overline{OC}}$ | $V_{\overline{OC}}$=5V | | 0.01 | | μA |
| $\overline{OC}$ Deglitch Time | $t_D$ | From Fault Condition to $\overline{OC}$ Assertion or De-assertion | | 7.5 | | ms |
| Under-Voltage Lockout | $V_{UVLO}$ | $V_{IN}$ Increasing | | 2.2 | | V |
| Under-Voltage Hysteresis | $\Delta V_{UVLO}$ | $V_{IN}$ Decreasing | | 0.2 | | V |
| Thermal Shutdown Threshold (Note2) | $T_{SD}$ | | | 150 | | °C |
| | $\Delta T_{SD}$ | Hysteresis | | 20 | | °C |

Note 2: Guarantee by design.

## Typical Performance Curves

$V_{IN}$= $V_{OUT}$=5V, $C_{IN}$=100µF, $C_{OUT}$=120µF, $R_{ILIM}$=20kΩ, TA=+25°C, unless otherwise noted. This is measured by using FP6861E-A1S6CTR.

**$I_{OUT}$=0A**

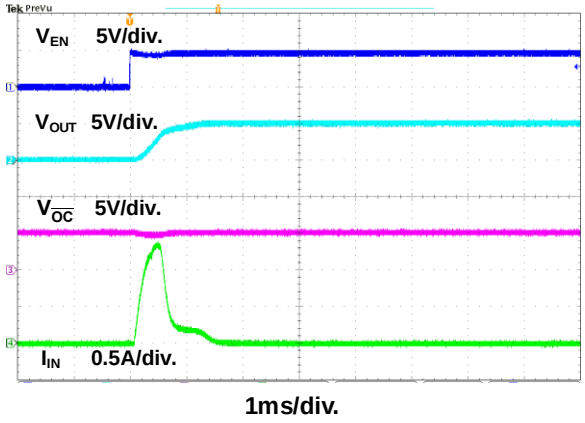



Figure 5. EN Start Up with No Load

**$I_{OUT}$=1A ($R_L$=5Ω)**

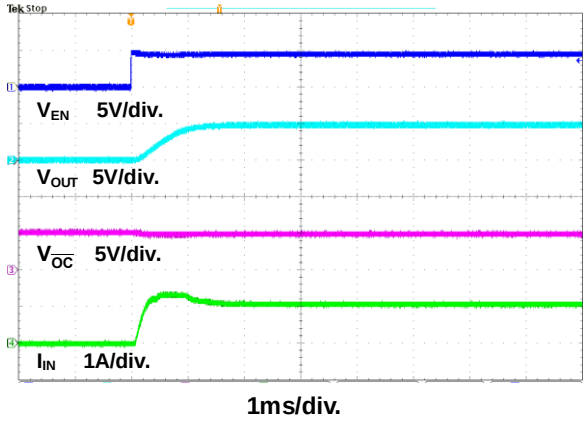



Figure 6. EN Start Up with Heavy Load

**$I_{OUT}$=0A**

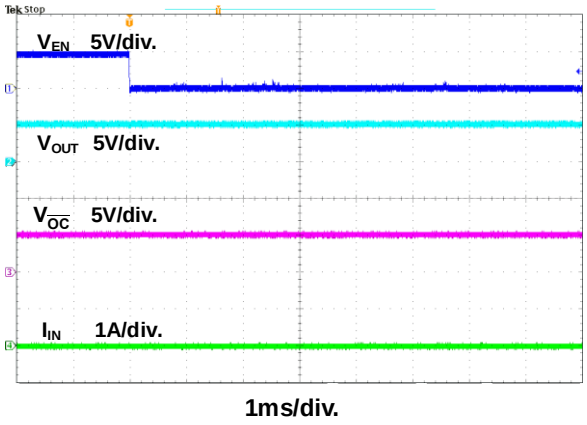



Figure 7. EN Power Off with No Load

**$I_{OUT}$=1A ($R_L$=5Ω)**

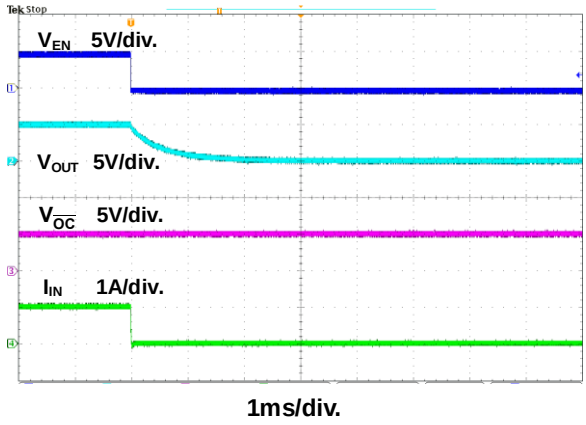



Figure 8. EN Power Off with Heavy Load

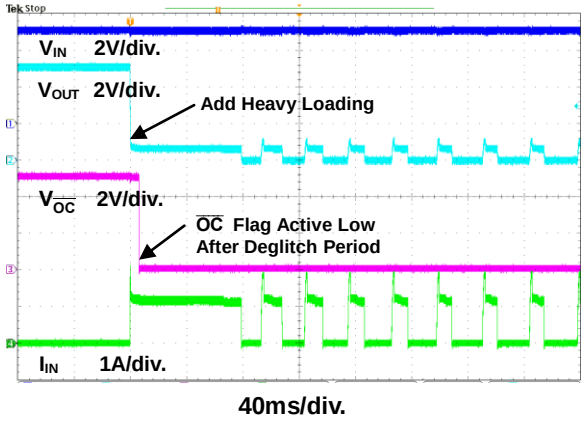



Figure 9. Short Heavy Loading Transient Response

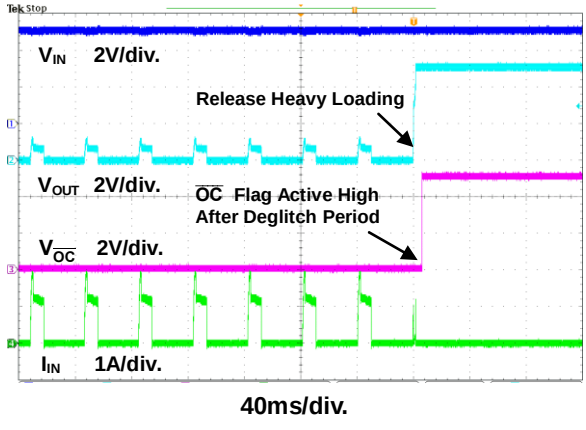



Figure 10. Release Heavy Loading Transient Response

## Typical Performance Curves (Continued)

$V_{IN}$= $V_{OUT}$=5V, $C_{IN}$=100µF, $C_{OUT}$=120µF, $R_{ILIM}$=20kΩ, TA=+25°C, unless otherwise noted. This is measured by using FP6861E-A1S6CTR.

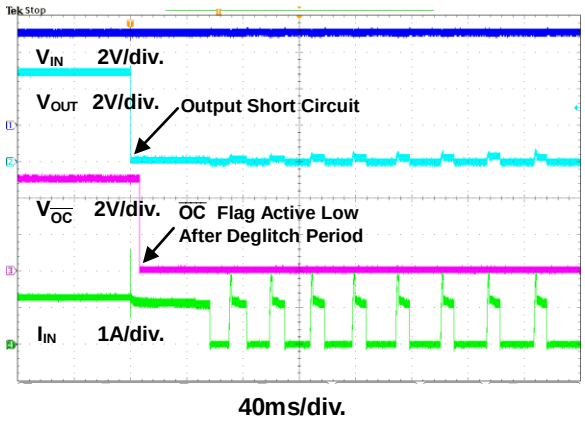



Figure 11. Heavy Loading to Short Circuit Transient Response

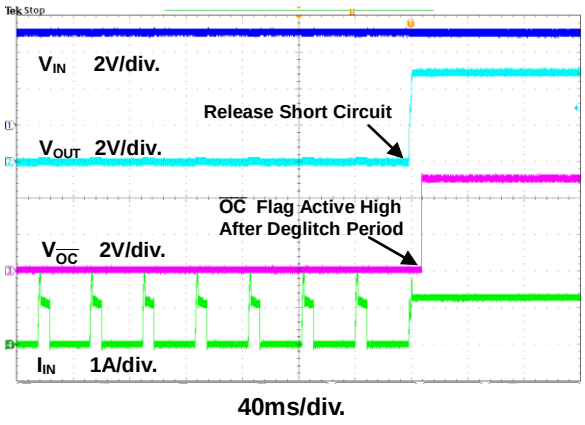



Figure 12. Short Circuit to Heavy Loading Transient Response

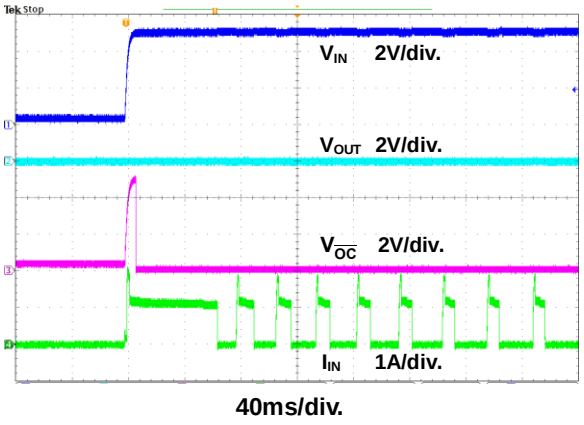



Figure 13. Short Circuit Response at Start Up

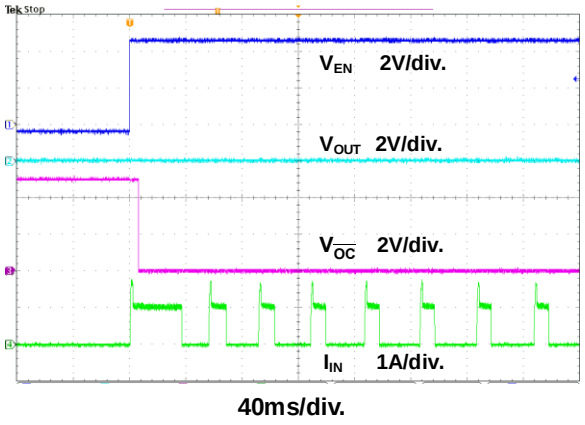



Figure 14. Short Circuit Response at Device Eable

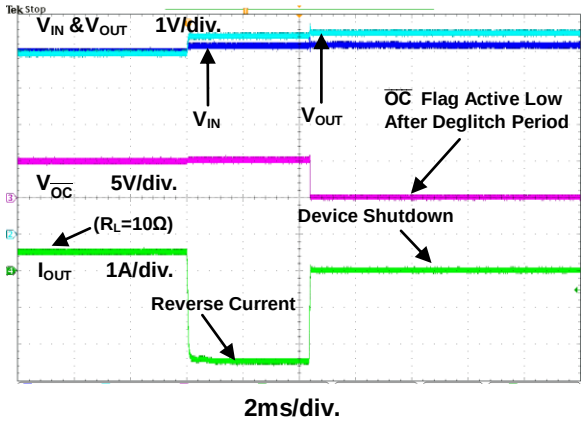



Figure 15. Reverse Voltage Protection Response

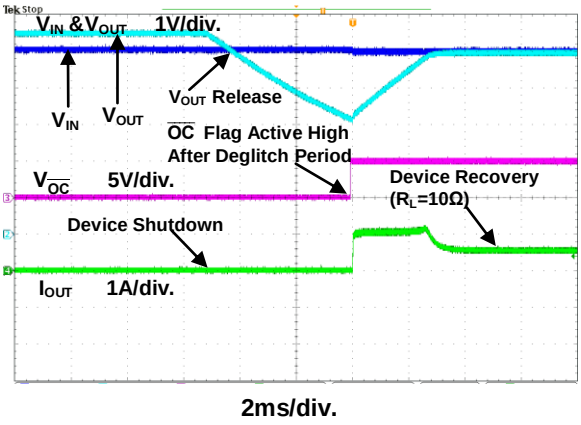



Figure 16. Reverse Voltage Protection Recovery

## Typical Performance Curves (Continued)

$V_{IN}$= $V_{OUT}$=5V, $C_{IN}$=100µF, $C_{OUT}$=120µF, $R_{ILIM}$=20kΩ, TA=+25°C, unless otherwise noted. This is measured by using FP6861E-A1S6CTR.

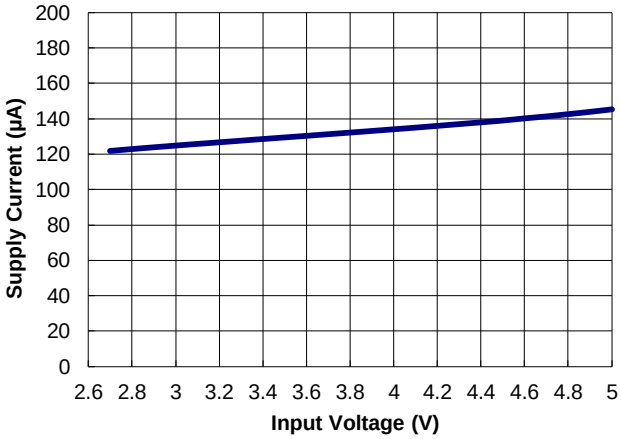



Figure 17. Supply Current vs. Input Voltage

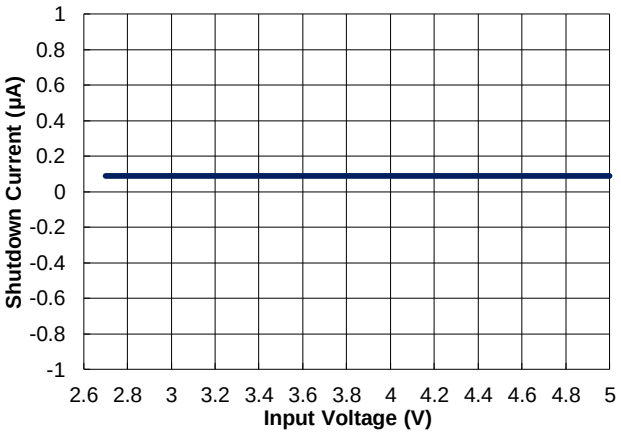



Figure 18. Shutdown Current vs. Input Voltage

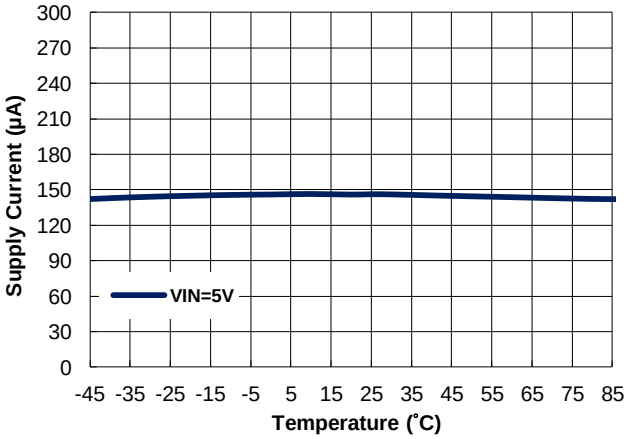



Figure 19. Supply Current vs. Temperature

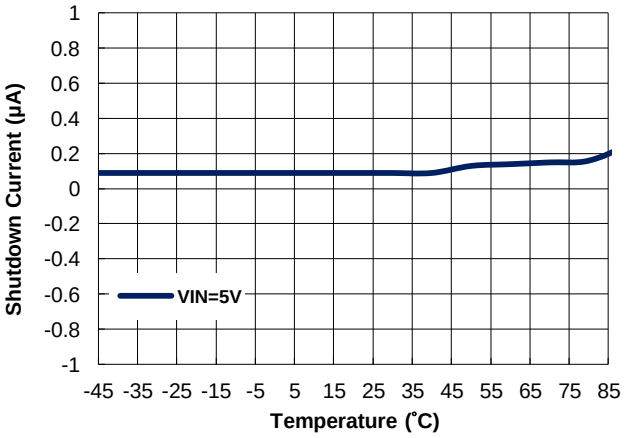



Figure 20. Shutdown Current vs. Temperature

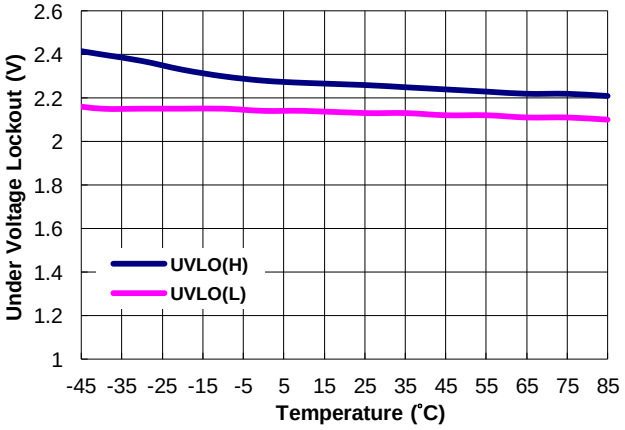



Figure 21. Under Voltage Lockout vs. Temperature

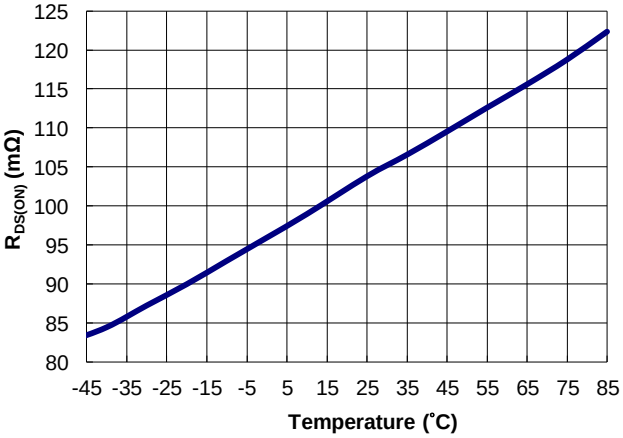



Figure 22. $R_{DS(ON)}$ vs. Temperature

## Application Information

The FP6861E-A/B is a single N-Channel MOSFET high-side power switch, optimized for self-powered and bus-powered Universal Serial Bus (USB) applications. The FP6861E-A/B operates from 2.7V to 6V input voltage range and provides low supply current. The switch's low $R_{DS(ON)}$, 100mΩ (for SOT-23-6 package), meets USB voltage drop requirements. It has one switch with enable control input. The switch has an error flag output to notify the USB controller when the current-limit, short-circuit or thermal-shutdown occurs.

### Under Voltage-Lockout

Under-voltage Lockout (UVLO) prevents the MOSFET switch from turning on until input voltage exceeds approximately 2.2V. If input voltage drops below approximately 2V, UVLO will turn off the MOSFET switch.

### Soft Start for Hot Plug-In Application

In order to eliminate the upstream voltage drop caused by the large inrush current during hot-plug events, the “soft-start” feature effectively isolates the power source from extremely large capacitive loads, satisfying the USB voltage drop requirements.

### Reverse Current Blocking

The USB specification does not allow an output device to source current back into the USB port. However, the FP6861E-A/B is designed to safely power noncompliant devices. When the device is disabled, the output will be switched to a high-impedance state, blocking reverse current flow from the output back to the input. The switch can pass the input to output when it is enabled.

### Reverse Voltage Protection

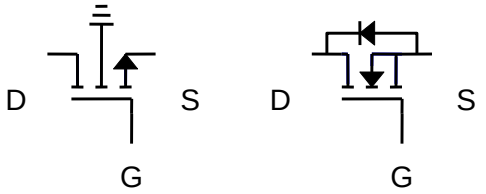
The reverse voltage protection will turn off N-channel MOSFET when output voltage is larger than input voltage 135mV for 4ms. Conversely, N-channel MOSFET will turn on when output voltage is lower than input voltage for 4ms.

### Supply Filter/Bypass Capacitor

The input capacitor must be at least 1μF low-ESR ceramic capacitor connected from VIN to GND, but can be increased without limit. Output short may cause sufficient ringing on the input (from source lead inductance) to destroy the internal control circuitry. The input transient must not exceed 6V of the absolute maximum supply voltage even for a short duration.

### Input and Output

VIN is the power source connection to the internal circuitry and the drain of the MOSFET. VOUT is the source of the MOSFET. In typical application, current flows through the switch from VIN to VOUT toward the load. If VOUT is greater than VIN, current will flow from VOUT to VIN since the MOSFET is bidirectional. There is no parasitic body diode between drain and source of the MOSFET, and the FP6861E-A/B will prevent reverse current flow if VOUT externally forces a higher voltage than VIN when the output is disabled.




FP6861E-A/B Normal MOSFET

### Output Filter Capacitor

Output is recommended to use a 22μF ceramic capacitor in parallel with a 100μF electrolytic capacitor. Standard bypass methods should be used to minimize inductance and resistance between the bypass capacitor and the downstream connector which reduce EMI and decouple voltage drop caused when downstream cables are hot-insertion transients. Ferrite beads in series with $V_{BUS}$, the ground line and the 0.1μF bypass capacitors at the power connector pins are recommended for EMI and ESD protection. The bypass capacitor should have a low dissipation factor to allow decoupling at higher frequencies.

### Error Flag

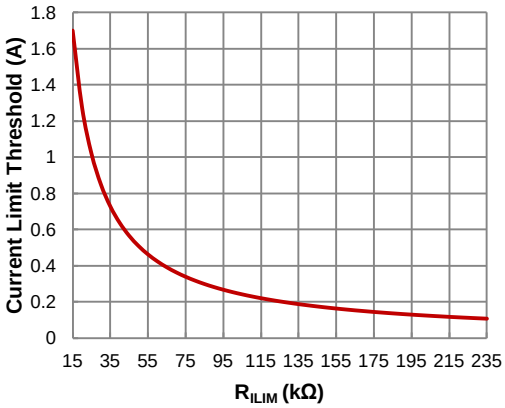
The FP6861E-A/B provides an open drain error flag output for the switch. For most applications, connect $\overline{OC}$ to VIN through a pull-up resistor. $\overline{OC}$ will go low when any following condition occurs:

1. The thermal shutdown occurs.
2. The switch is in current limit or short circuit conditions.
3. Reverse voltage protection occurs when output voltage exceeds the input voltage.

## Application Information (Continued)

### Adjustable Current Limit

The current limit circuitry prevents damage to the MOSFET switch but can deliver load current up to the current limit threshold through the switch. FP6861E-A/B provides adjustable current limit threshold between 0.12~1.7A through an external resistor. The current limit threshold(Typ.) and $R_{ILIM}$ curve is show below：




Designer can use following equation to easy calculate the value of the external resistor for porposed typical current limit value：

$$I_{LIM(Typ.)}(mA)=\frac{25500}{R_{ILIM}(k\Omega)} \quad | 15k\Omega \leq R_{ILIM} \leq 235k\Omega$$

However, the curve graph and equation does not include the external resistor tolerance. The table1 shows a process that accounts for worst case resistor tolerance assuming 1% resistor range for external resistor($R_{ILIM}$).

| Design Current Limit (mA) | Ideal $R_{ILIM}$ Value (kΩ) | 1% Tolance Real $R_{ILIM}$ (kΩ) | Actual Limits (with $R_{ILIM}$ tolerance) | | |
|---|---|---|---|---|---|
| | | | $I_{LIM}$ Min. (mA) | $I_{LIM}$ Typ. (mA) | $I_{LIM}$ Max. (mA) |
| 120 | 212.50 | 213 | 92.03 | 119.72 | 148.66 |
| 200 | 127.50 | 129 | 158.65 | 197.67 | 240.41 |
| 300 | 85.00 | 85.6 | 245.65 | 297.90 | 353.64 |
| 400 | 63.75 | 64.2 | 333.81 | 397.20 | 463.59 |
| 500 | 51.00 | 51.1 | 425.75 | 499.02 | 574.64 |
| 600 | 42.50 | 42.7 | 515.58 | 597.19 | 680.44 |
| 700 | 36.43 | 36.5 | 609.43 | 698.63 | 788.69 |
| 800 | 31.88 | 32 | 701.20 | 796.88 | 892.64 |
| 900 | 28.33 | 28.4 | 796.33 | 897.89 | 998.74 |
| 1000 | 25.50 | 25.5 | 893.22 | 1000.00 | 1105.27 |
| 1100 | 23.18 | 23.2 | 987.91 | 1099.14 | 1208.09 |
| 1200 | 21.25 | 21.3 | 1082.12 | 1197.18 | 1309.24 |
| 1300 | 19.62 | 19.6 | 1182.46 | 1301.02 | 1415.83 |
| 1400 | 18.21 | 18.2 | 1279.66 | 1401.10 | 1518.08 |
| 1500 | 17.00 | 16.9 | 1384.85 | 1508.88 | 1627.73 |
| 1600 | 15.94 | 15.8 | 1487.86 | 1613.92 | 1734.15 |
| 1700 | 15.00 | 15 | 1572.59 | 1700.00 | 1821.05 |

Table1. Common $R_{ILIM}$ Resistor Selections Guide

## Application Information (Continued)

### Short-Circuit Protection Mode

When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once exceeds the current limit threshold, FP6861E-A will enter constant current mode until the thermal shutdown occurs or the fault is removed. When power MOSFET turns off, FP6861E-B will enter latch-off mode until power restart or EN reset.

### Power Dissipation

The device's junction temperature depends on several factors, such as the load, PCB layout, ambient temperature and package type. However, the maximum output current must be decreased at higher ambient temperature to ensure the junction temperature does not exceed 125°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the $R_{DS(ON)}$ of switch as below:

$$P_D = R_{DS(ON)} \times (I_{OUT})^2$$

Although the devices are rated by current limit, but the application may limit the amount of output current based on the total power dissipation and the ambient temperature. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature 125°C, $T_A$ is the ambient temperature and the $\theta_{JA}$ is the junction to ambient thermal resistance.

The junction to ambient thermal resistance $\theta_{JA}$ is related to layout. For SOT-23-6 package, the thermal resistance $\theta_{JA}$ is 250°C/W on the standard JEDEC 51-3 single-layer thermal test board.

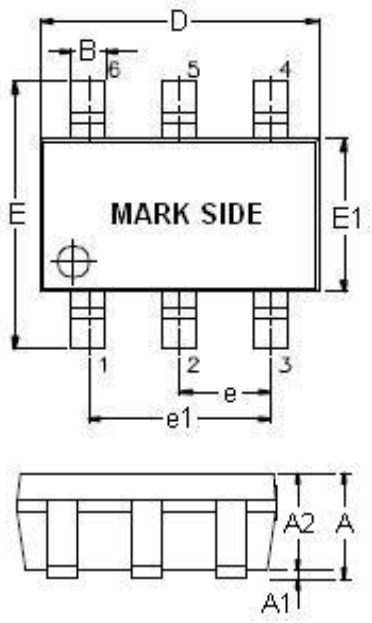
### PCB Layout

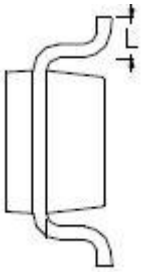
In order to meet the voltage drop and EMI requirements, careful PCB layout is necessary. The following guidelines must be considered:

1. Keep all $V_{BUS}$ traces as short as possible, and use at least 50-mil and 2 ounce copper for all $V_{BUS}$ traces.
2. Locate the FP6861E-A/B as close to the output port as possible to limit switching noise.
3. Locate the ceramic bypass capacitors as close to the VIN pins of the FP6861E-A/B as possible.
4. Avoid vias as much as possible. If vias are necessary, make them as large as feasible.
5. Place a ground plane under all circuitry to lower both resistance and inductance, and improve DC and transient performance (use a separate ground and power plans if possible).
6. Place cuts in the ground plane between ports to help reducing the coupling of transients between ports.
7. Locate the output capacitor and ferrite beads as close to the USB connectors as possible to lower impedance (mainly inductance) between the port and the capacitor, and improve transient load performance.

## Outline Information

**SOT-23-6 Package (Unit: mm)**

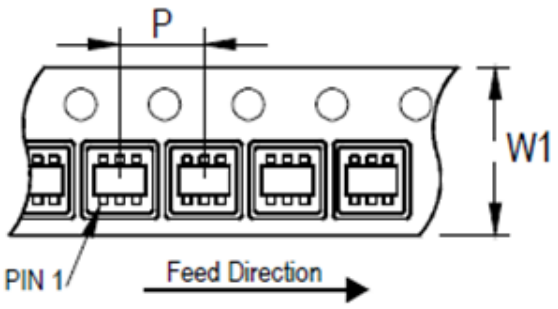


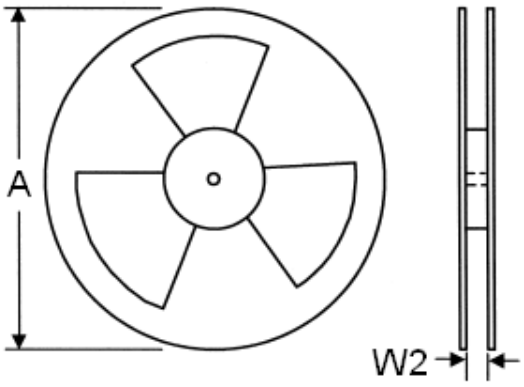




| SYMBOLS UNIT | DIMENSION IN MILLIMETER | |
|---|---|---|
| | MIN | MAX |
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| B | 0.30 | 0.50 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.70 |
| e | 0.90 | 1.00 |
| e1 | 1.80 | 2.00 |
| L | 0.30 | 0.60 |

Note：Followed From JEDEC MO-178-C.

## Carrier Dimensions

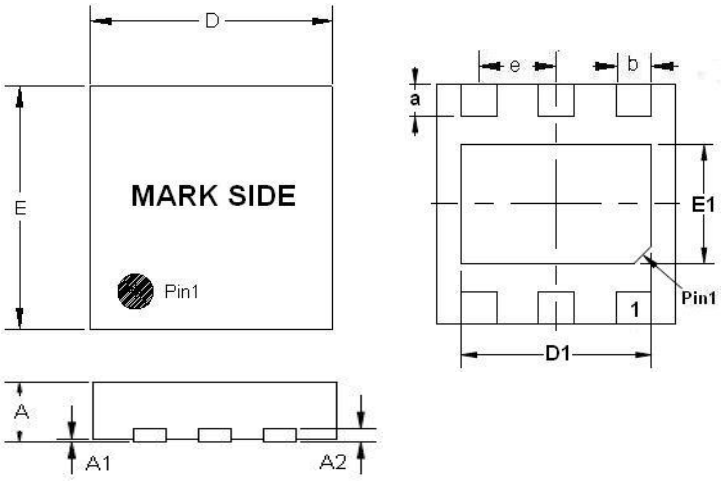



| Tape Size (W1) mm | Pocket Pitch (P) mm | Reel Size (A) | | Reel Width (W2) mm | Empty Cavity Length mm | Units per Reel |
|---|---|---|---|---|---|---|
| | | in | mm | | | |
| 8 | 4 | 7 | 180 | 8.4 | 300~1000 | 3,000 |

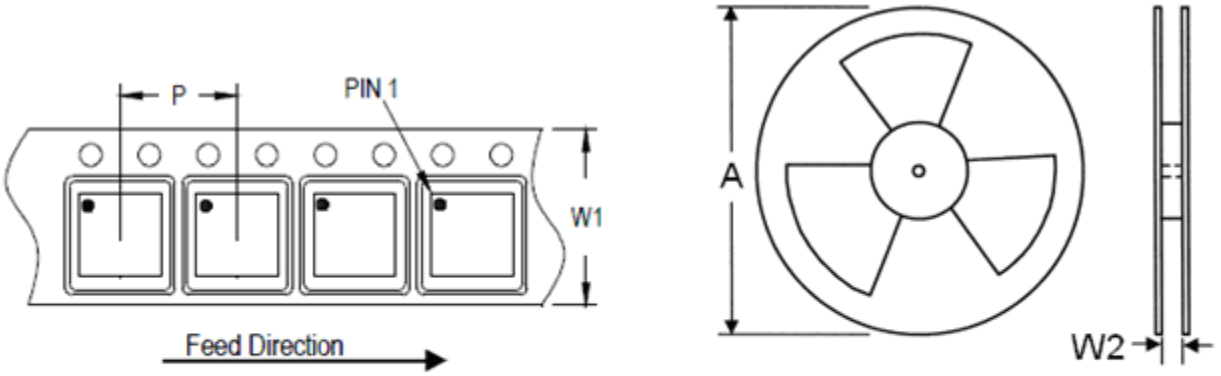
## Outline Information (Continued)

**TDFN-6 (2mm×2mm) (pitch: 0.65mm)Package (Unit: mm)**




| SYMBOLS UNIT | DIMENSION IN MILLIMETER | |
|---|---|---|
| | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A2 | 0.19 | 0.22 |
| D | 1.95 | 2.05 |
| E | 1.95 | 2.05 |
| a | 0.20 | 0.40 |
| b | 0.25 | 0.35 |
| e | 0.60 | 0.70 |
| D1 | 1.15 | 1.65 |
| E1 | 0.55 | 1.05 |

## Carrier Dimensions




| Tape Size (W1) mm | Pocket Pitch (P) mm | Reel Size (A) | | Reel Width (W2) mm | Empty Cavity Length mm | Units per Reel |
|---|---|---|---|---|---|---|
| | | in | mm | | | |
| 8 | 4 | 7 | 180 | 8.4 | 400~1000 | 3,000 |